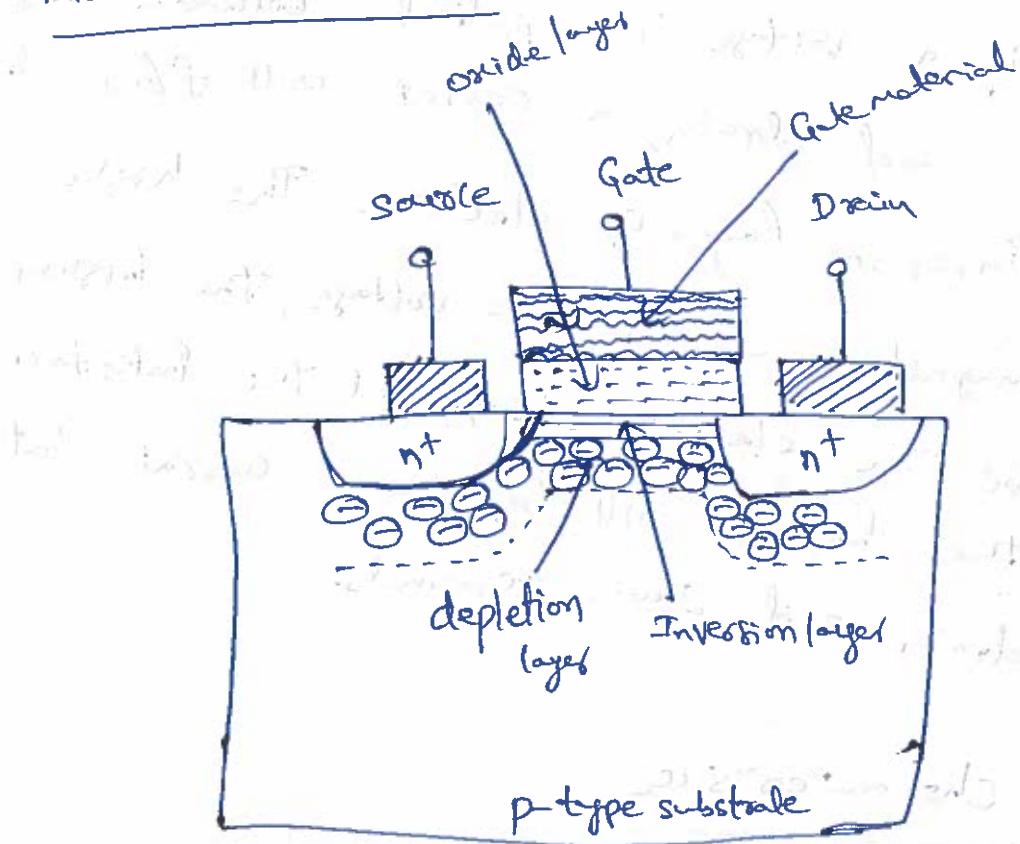


### UNIT-III

#### MOSFET Circuits:

##### MOSFET structure:

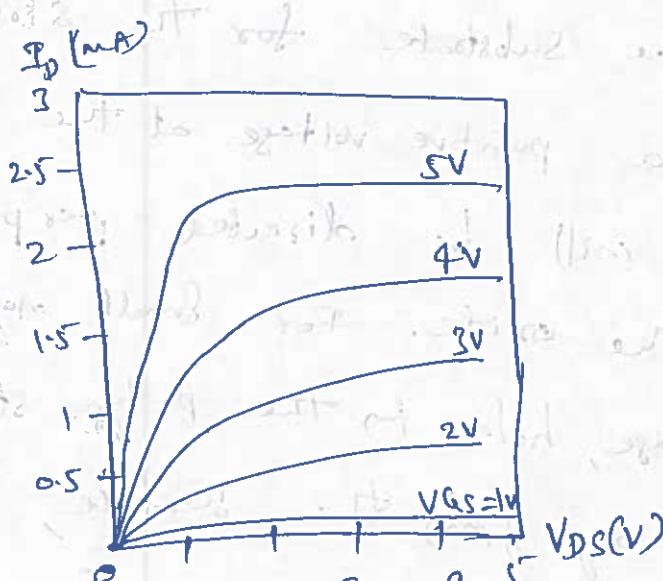


If we ground the substrate for the structure in fig and apply a positive voltage at the gate, an electric field will be directed perpendicular through the oxide. For small magnitude of the gate voltage, holes in the p-type structure will be repelled away from the surface, leaving behind negative acceptor ions. As the magnitude of the gate voltage increases, electrons

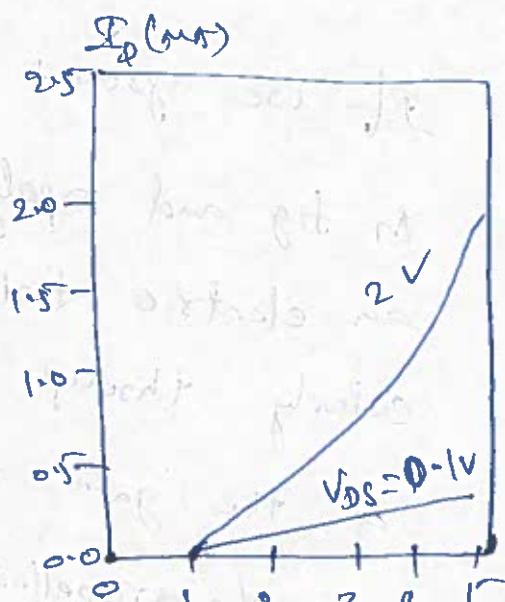
will gradually start accumulating at the silicon-oxide interface, and form a layer of negative charges, called an inversion layer.

Now if a voltage is applied between the source and drain, a current will flow, due to the inversion layer of electrons. The higher the magnitude of the gate voltage, the higher will be the electron charge at the interface and the higher will be the current between the drain and source terminals.

### I-V Characteristics:



(a)



(b)

Fig (a) Drain characteristics of an NMOSFET  
 (b) Transfer Characteristics.

As  $V_{GS}$  is made more positive, the current  $I_D$  increases slowly at first, and then much more rapidly with an increase in  $V_{GS}$ .

The threshold voltage ( $V_T$ ) of a MOSFET is defined as the gate-source voltage at which the ~~the~~ drain current per unit width reaches some defined small value, say  $10\text{mA}$ ,

The magnitude of  $V_T$  for MOSFETs ranges between 0.5 and 5V, depending on the channel length and oxide thickness.

### MOSFET as a Switch!

The p-channel devices will have more than twice the on resistance of an equivalent n-channel device of the same geometry and under the same operating conditions.

The smaller size of the n-channel CMOS also makes it faster while performing switching functions, and gives it a higher bandwidth.

In small signal applications,

switching functions based on the current-voltage characteristics into three regions of operation.

For an NMOS transistor

Cut off region → (OFF)

for  $V_{GS} < V_T \rightarrow (\text{OFF})$

$$I_D = 0$$

for  $V_{GS} > V_T$

Triode, or linear, region

$$I_D = \frac{\mu_n C_{ox} W}{L} \left( V_{GS} - V_T - \frac{1}{2} V_{DS} \right) V_{DS} \text{ if } V_{DS} \leq (V_{GS} - V_T)$$

Saturation region: (ON)

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_T)^2 \text{ if } V_{DS} \geq (V_{GS} - V_T)$$

Here,  $\mu_n$  is the electron mobility,

$C_{ox}$  is the gate-oxide capacitance per unit area

$W$  is the width of the channel

$L$  is the length of the channel.

$I_D$  is the current entering the drain terminal.

$$V_G > V_T \rightarrow (\text{ON})$$

(B)

### Small Signal equivalent circuit

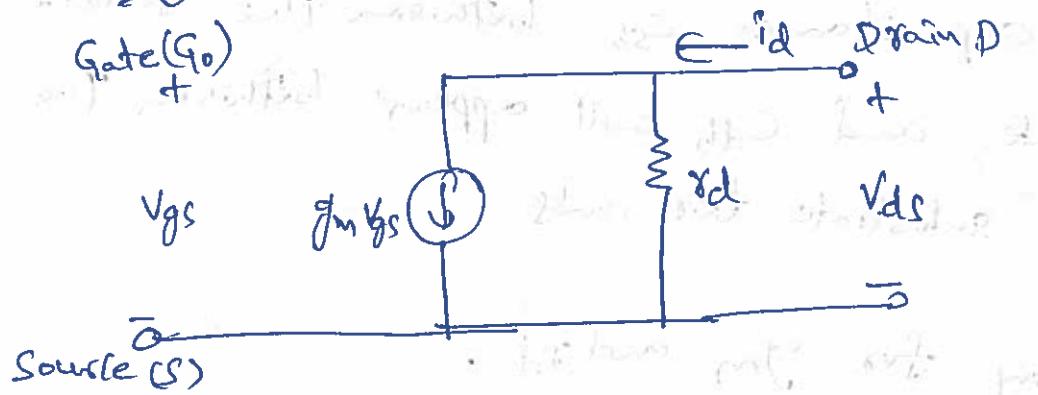


Fig (a) The low-frequency small -

signal MOSFET model.

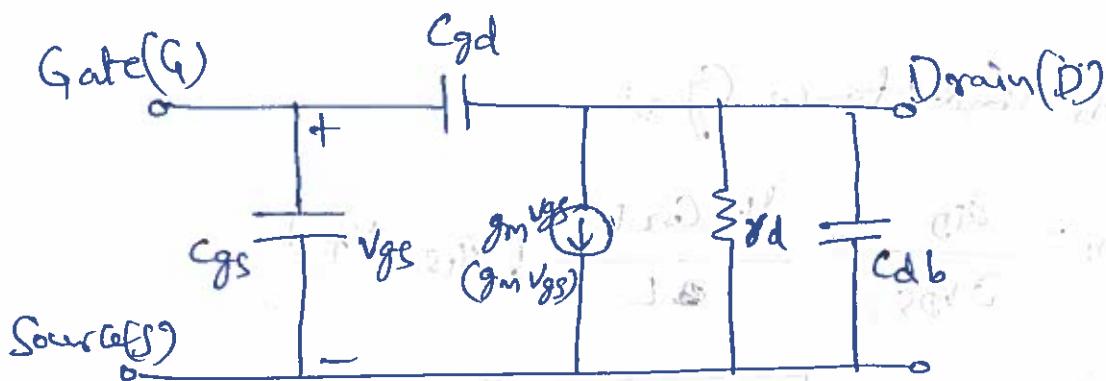


Fig (b). The high-frequency model taking node capacitors into account.

- If the small resistances of the source and drain region are neglected, the small-signal equivalent circuits of the MOSFET are shown in fig.
- The high frequency model of fig(b) is shown with the substrate terminal shorted to the source.

If this is not the case, then there will be one more capacitance,  $C_{SB}$  between the source and substrate, and  $C_{DB}$  will appear between the drain and substrate terminals.

expression for  $g_m$  and  $r_d$ .

In ~~saturation~~ Using eqn,

$$I_D = \frac{4\mu_n C_o x W}{2L} (V_{GS} - V_T)^2 \text{ if } V_{DS} \leq (V_{GS} - V_T)$$

transconductance ( $g_m$ )

$$g_m = \frac{\partial I_D}{\partial V_{DS}} = \frac{4\mu_n C_o x W}{2L} (V_{GS} - V_T)$$

$$= \sqrt{2 \frac{\mu_n C_o x W}{L} I_D}$$

$$= \frac{2 I_D}{(V_{GS} - V_T)}$$

→ Gain, Input and output impedances small - ⑨

Signal model and Common source.

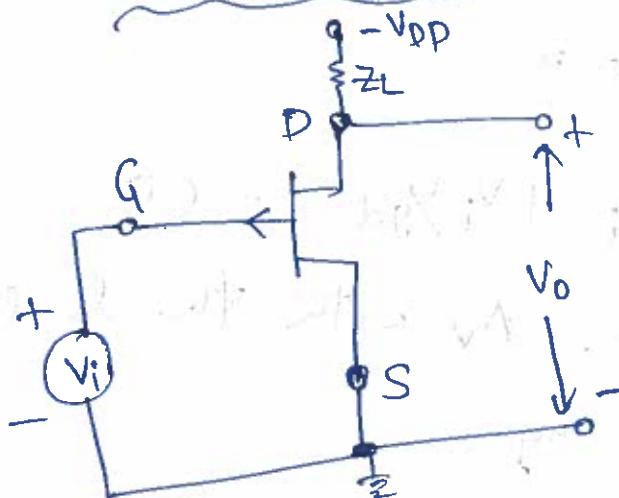


Fig (a) The Common-Source amplifier circuit

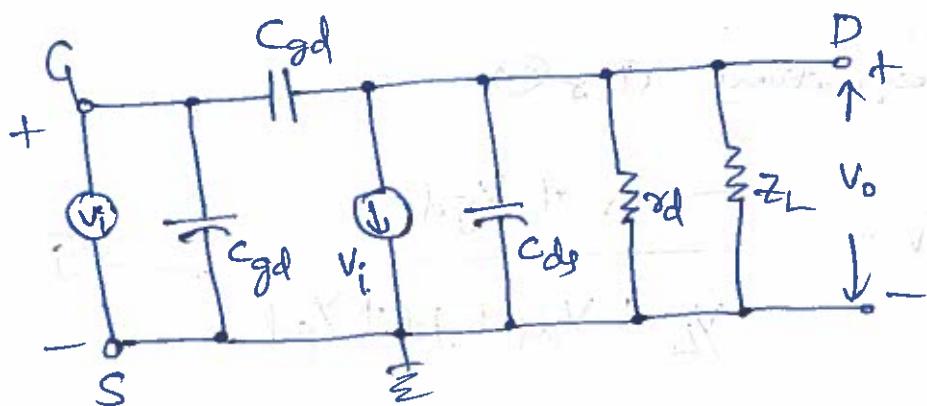


Fig (b) Small-signal equivalent circuit at high frequency.

Voltage gain:

$$y = \frac{1}{Z} = Y_L + Y_{ds} + g_d + Y_{gd} \quad ①$$

where  $Y_L = \frac{1}{Z_L}$  = admittance corresponding to  $Z_L$

$Y_{ds} = j\omega C_{ds}$  = admittance corresponding to  $C_{ds}$

$g_d = \frac{1}{r_d}$  Conductance corresponding to  $r_d$

$Y_{gd} = j\omega C_{gd}$  = admittance corresponding to  $C_{gd}$

The current for the direction from D to S for a zero-resistance wire connecting the output terminals is

$$I = -g_m V_i + V_i Y_{gd} \quad \text{--- (1)}$$

The amplification  $A_v$  with the load  $Z_L$  in place is given by

$$A_v = \frac{V_o}{V_i} = \frac{I_Z}{V_i} = \frac{I}{V_i Y} \quad \text{--- (2)}$$

From equations (1) & (2)

$$A_v = \frac{-g_m + Y_{gd}}{Y_L + Y_{gd} + g_d + Y_{gd}} \quad \text{--- (3)}$$

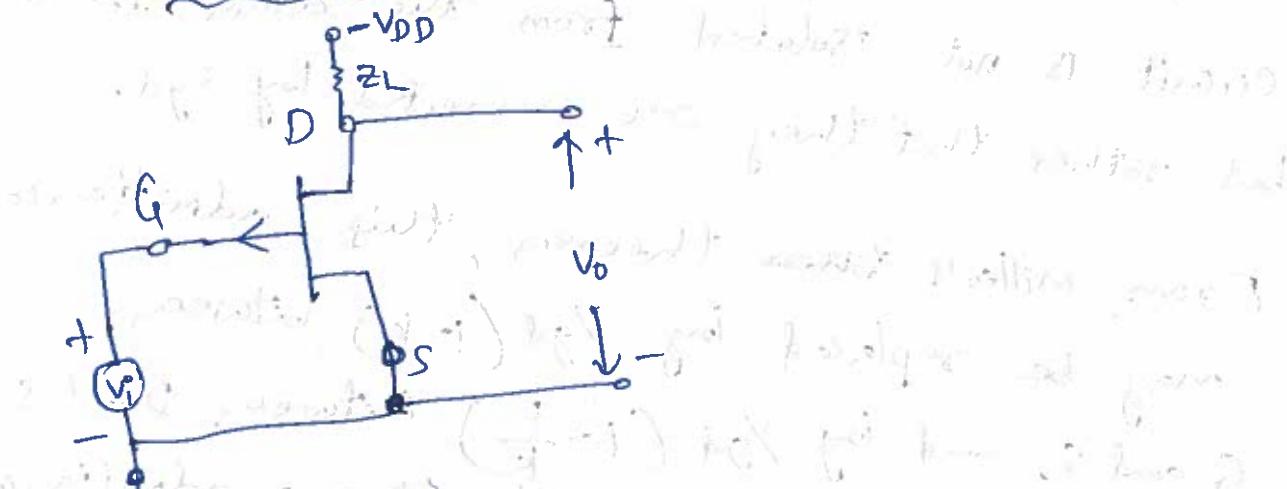
At low frequencies the FET capacitance can be neglected and hence

$$Y_{ds} = Y_{gd} \approx 0$$

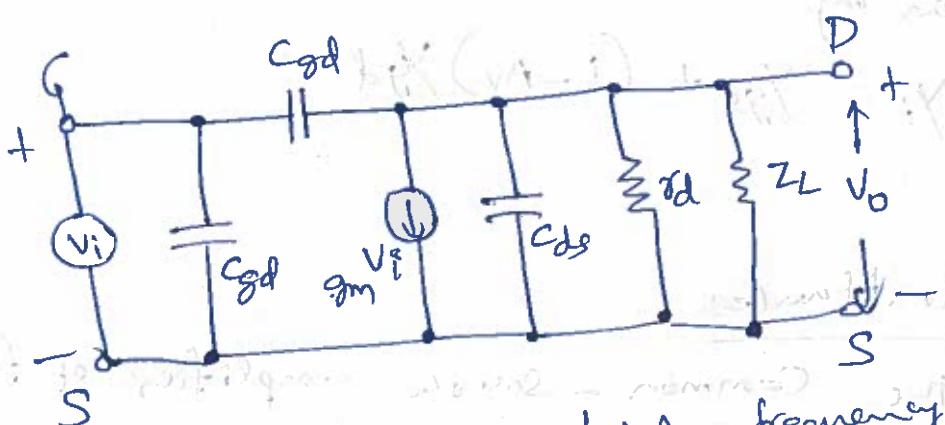
Under these conditions eqn (3) reduced to

$$A_v = \frac{-g_m}{Y_L + g_d} = \frac{-g_m r_d Z_L}{r_d + Z_L} = -g_m Z_L'$$

Gain, input and output impedances, small-signal model and Common-drain amplifier:



fig(a) The Source-follower



fig(b) Small-signal high-frequency equivalent circuit

Voltage Gain: The output voltage  $V_O$  can be found from the product of the short-circuit current and the impedance between terminals S and N.

We now find for the voltage gain

$$AV \approx \frac{gmR_s}{1 + (gm + gd)R_s}$$

Input admittance:

### Input Admittance:-

An inspection of fig(b) reveals that the gate circuit is not isolated from the drain circuit, but rather that they are connected by  $y_{gd}$ .

From Miller's ~~rule~~ theorem, this admittance may be replaced by  $y_{gd}(1-k)$  between D and S, G and S, and by  $y_{gd}(1-\frac{1}{k})$  between D and G where  $k = A_v$ . Hence the input admittance is given by

$$y_i = y_{gs} + (1 - A_v) y_{gd}$$

### Output Admittance

from the Common-Source amplifier of fig(1) the output impedance is obtained by "looking into the drain" with the input voltage set equal to zero. If  $v_i = 0$  in fig(b), we see  $r_d$ ,  $c_{ds}$ , and  $y_{gd}$  in parallel. Hence the output admittance with  $Z_L$  considered external to the amplifier is given by

$$y_o = y_{gd} + y_{ds} + y_{gd}$$

UNIT-3FET'S : JFET

The FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence the name field effect Transistor (FET). As current conduction is only by majority carriers.

Based on the construction, The FET can be classified into two types of Junction FET (JFET) and metal oxide semiconductor FET (MOSFET)

depending up on the majority carriers, JFET

has been classified into two types namely,

1) N-channel JFET, with electrons as the majority

carriers

2) p-channel JFET with holes as the majority carriers

Construction of N-channel JFET

It consists of a N-type bar, which is made of silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called Source and

Drain.

Source (S): This terminal is connected to the negative pole of the battery. Electrons are the majority carriers so the N-type bar enter the bar through this terminal.

Drain (D): This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G): Heavily doped p-type silicon is diffused on both sides of the N-type Silicon bar by which PN junctions are formed. These layers are joined together and called Gate (G).

Channel: The region BC of the N-type bar between the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference  $V_{DS}$  is applied between the source and drain.

## principle of operation:

- when  $V_{GS} = 0$  and  $V_{DS} = 0$ , when no voltage is applied between drain and source, and gate and source, the thickness of the depletion region around the pn junction is uniform as shown in fig. ①
- when  $V_{DS} = 0$  and  $V_{GS}$  is decreased from zero. In this case, the pn junctions are reverse biased and hence the thickness of the depletion region increases.
- when  $V_{GS} = 0$  and  $V_{DS}$  is increased from zero. Drain is positive with respect to the source with  $V_{GS} = 0$ . Now the majority carriers (electrons) flow through the n-channel from source to drain. Current  $I_D$  flows from drain to source. The current will depend upon the following factors.
1. The number of majority carriers (electrons) available for the channel
  2. The length  $L$  of the channel
  3. Area of the channel at B.
  4. The magnitude of the applied voltage  $V_{DS}$ .

V-I characteristics

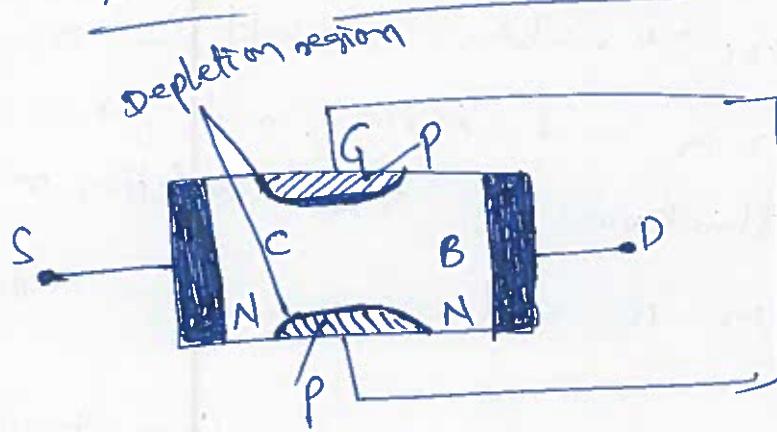


Fig: JFET Construction

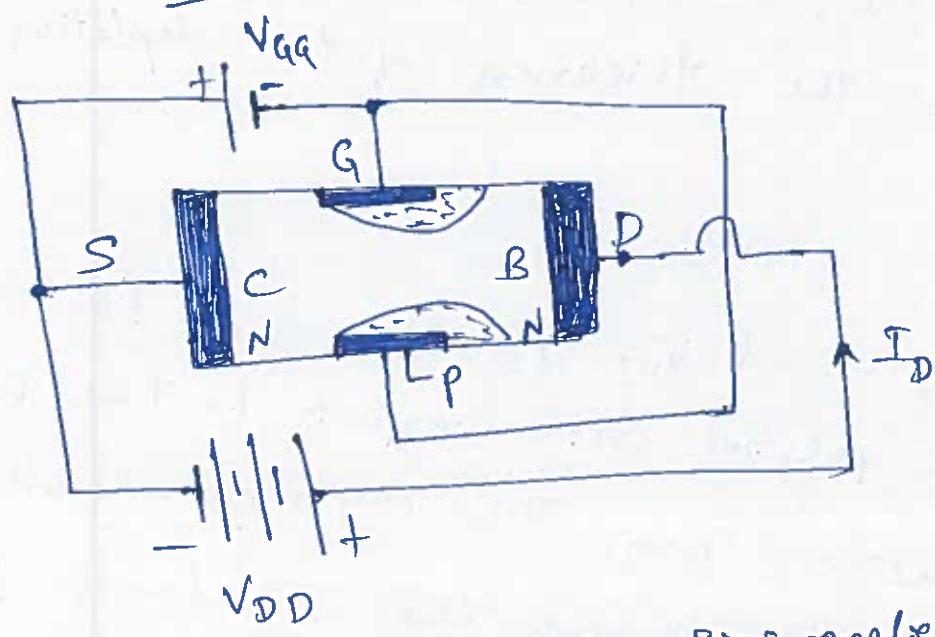


Fig: JFET under ~~reverse~~-Applied Bias

Digital Circuits:Digital (binary) operations of system:

- A digital system functions in a binary manner.
- exist only in two having two possible states i.e. 0 or 1 high to low
- A node may be at a high voltage ~~voltage~~ ~~volt~~ or low voltage of  $4 \pm 1\text{V}$  (GND) at a low voltage of  $0.2 \pm 0.2\text{V}$ , but no other values are allowed.

Binary state terminology:

	1	2	3	4	5
one of the states--	True	High	1	off	Closed
The other state.	False	Low	0	on	open

ex: decimal system:

$$\begin{aligned}
 1,264 &= 1 \times 10^3 + 2 \times 10^2 + 6 \times 10^1 + 4 \times 10^0 \\
 &= 1000 + 200 + 60 + 4 \\
 &= \underline{\underline{1,264}}
 \end{aligned}$$

ex: in binary system: base is 2

$$\begin{aligned}
 10011 &= 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \\
 &= 16 + 0 + 0 + 2 + 1 \\
 &= \underline{\underline{19}}
 \end{aligned}$$

→ Equivalent numbers by decimal and binary notation

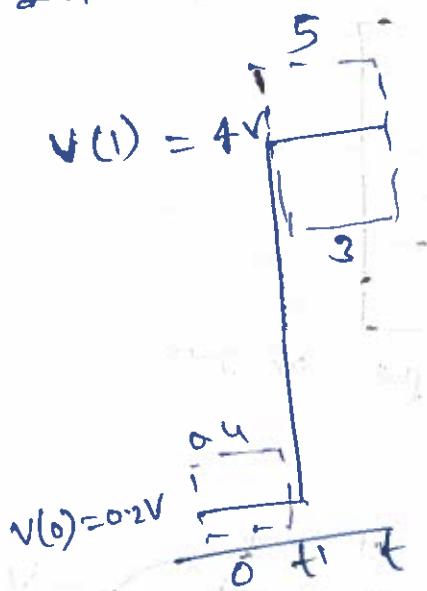
Decimal notation	Binary notation	Decimal notation	Binary notation
0	00000	11	01011
1	00001	12	01100
2	00010	13	01101
3	00011	14	01110
4	00100	15	01111
5	00101		10000
6	00110	16	1
7	00111	17	10001
8	01000	18	10010
9	01001	19	10011
10	01010	20	10100
		21	10101

A binary digit (1 or 0) is called a bit

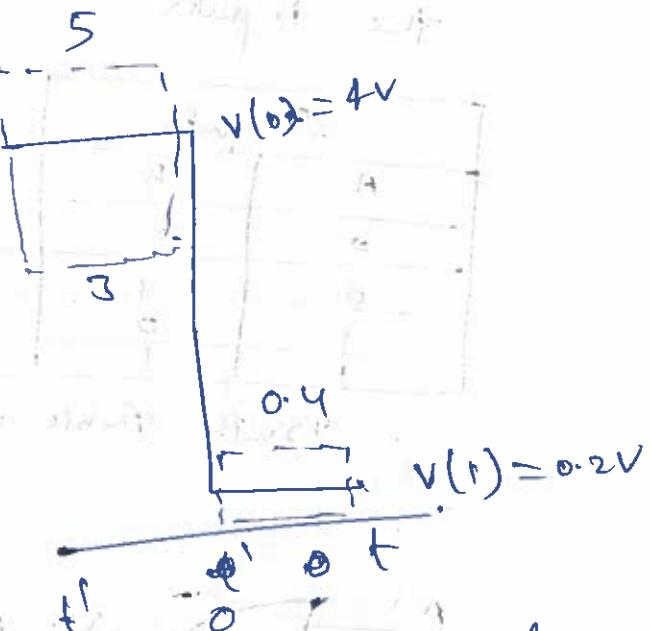
A group of bits called a byte, word (or) code

## Logic Systems:

In a static logic system a bit is implemented as one of two voltage levels, more ~~is~~ positive voltage is the 1 level and the other is the 0 level. This is called positive logic in a negative logic system, more negative voltage state of the bit is as the 1 level and the more positive of the 0 level.



(a) positive logic



(b) negative logic

## D) OR Gate

- The OR gate performs logical addition.
- An OR gate has two or more inputs and one output.
- An OR gate produces a High on the output when any of the input is High.
- The output is Low only when all of the inputs are Low.

Inputs		Output
A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

Truth table for 2-input OR gate



Fig: Two inputs of gate

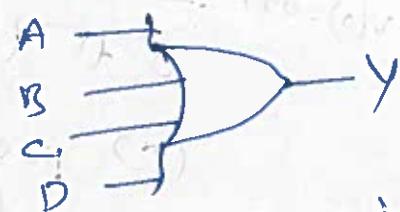
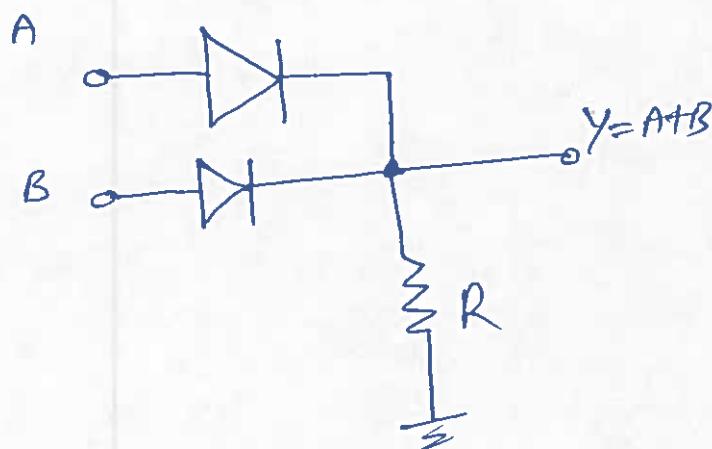
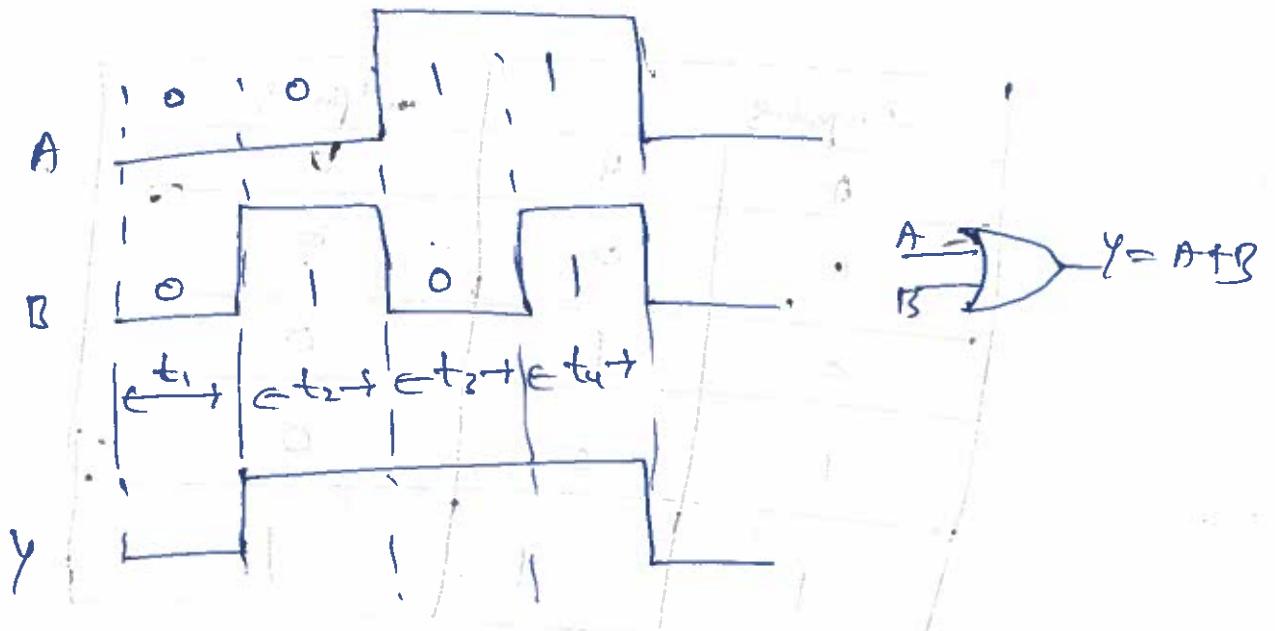


Fig four inputs OR gate



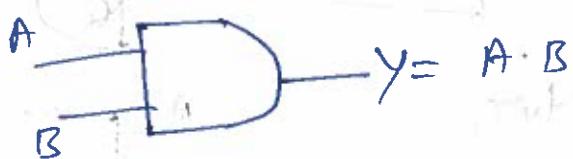
figs 2-input OR gate  
with diode circuit



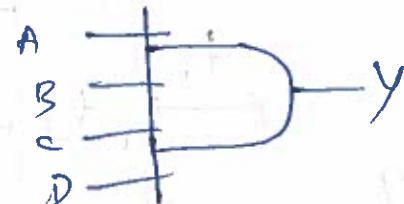
Sig: operation of an OR gate with pulsed inputs.

## 2) AND gate!

- AND gate performs logical multiplication.
- The AND gate may have two or more inputs and single output.
- The output is HIGH only when all of the inputs are HIGH.
- When ~~is~~ any of the inputs are LOW, the output is LOW.



Sig: Two inputs to AND gate



Sig: Four inputs to AND gate

Inputs		Output
A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

Truth table for 2 input AND gate

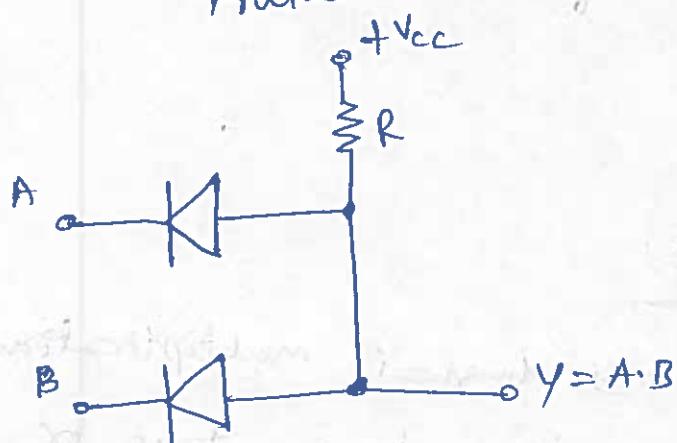
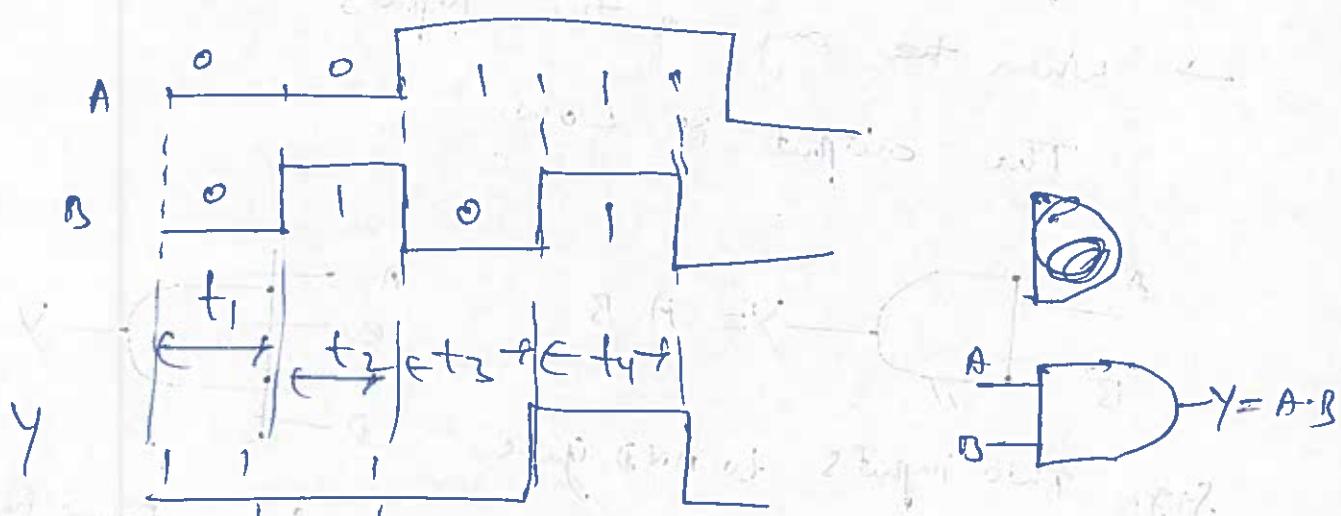


fig: 2 - input AND gate  
using diode

pulsed operation:



figs Timing Diagrams for 2 input AND gate

### 3) NOT gate (or) Inverter

- The Inverter (or) NOT gate changes one logic level to its opposite level.  
i.e. it changes a logic 1 to a logic 0 and a logic 0 to a logic 1.



Inverter (or) NOT gate symbol.

The bubble [o] is inversion indicator.

- When a HIGH Level is applied to an inverter input, a Low level will appear on its output.
- When a Low level is applied to its input, a HIGH level will appear on its output.

Inputs	Output	Inputs	Output
Low	HIGH	0	1
HIGH	Low	1	0

Table: NOT gate Truth Table

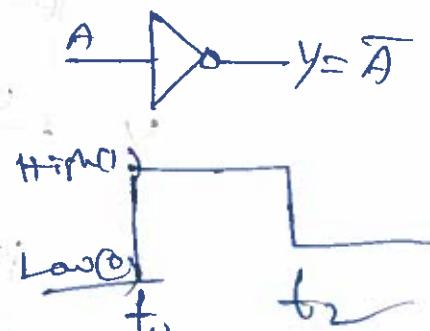
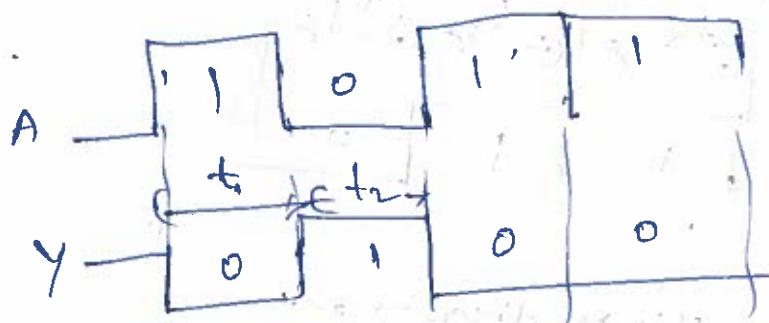


Fig & timing diagram for NOT gate

## The Exclusive OR Gate (OR EX-OR gate)

- An EX-OR gate has two or more inputs and one output.
- The output is HIGH only when odd number of inputs are HIGH.



$$y = \overline{AB} + \overline{A}\overline{B}$$

1 0 + 0 1

fig: two input EX-OR

Inputs		Output
A	B	y
0	0	0
0	1	1
1	0	1
1	1	0

table: Truth table for 2-input EX-OR gate



If  $A=1$  and  $B=0$ , or if  $B=1$  and  $A=0$ , then  $y=1$ . In both cases,

Then  $y=1$  then Boolean expression

$$y = AB + \overline{A}\overline{B}$$

A  $\overline{A}$  B  $\overline{B}$   $\overline{AB}$   $\overline{A}\overline{B}$   $y = (AB) + (\overline{AB})$

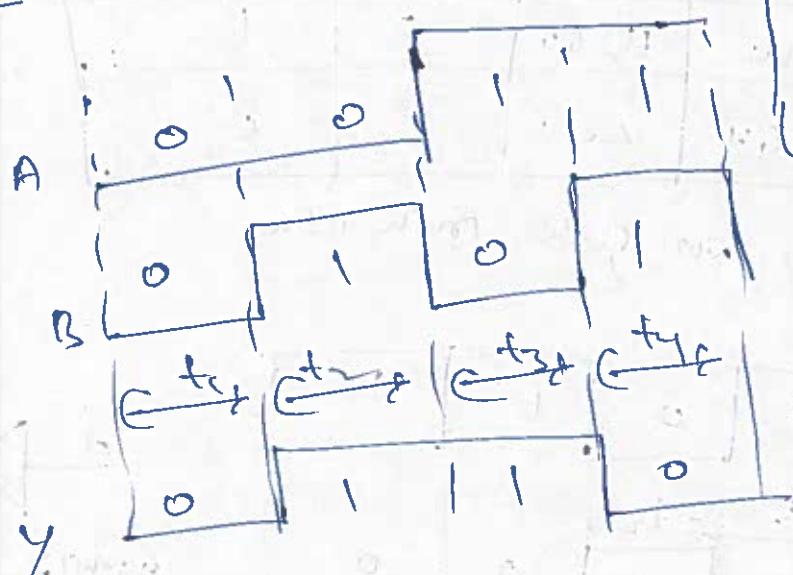


fig: Timing diagram for 2-input EX-OR gate

## DeMorgan's Theorems:

1)  $\overline{AB} = \overline{A} + \overline{B}$

The complement of a product is equal to the sum of the complements.

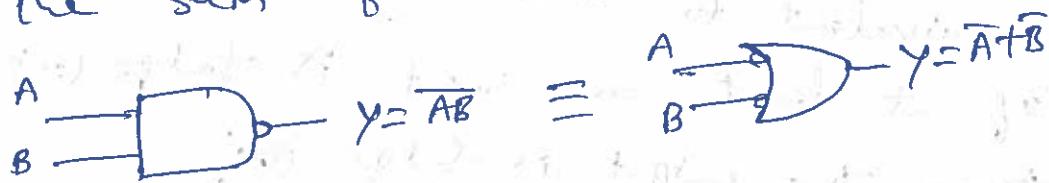


fig: Demorgan's theorem.

Truth table

A	B	$\overline{AB}$	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	0	0
1	1	0	0

2)  $\overline{A+B} = \overline{A}\overline{B}$

The complement of a sum is equal to the product of the complements.

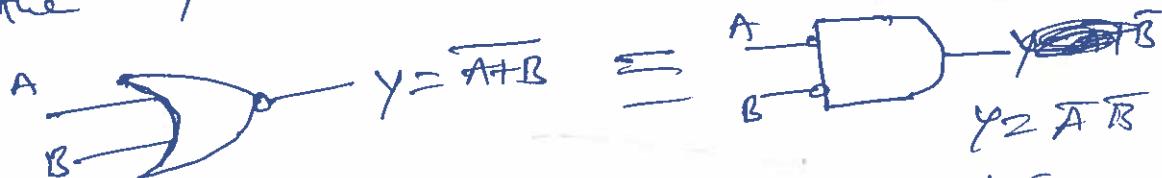


fig: combinational logic circuit (a)  
Demorgan's theorem.

Truth table

A	B	$\overline{A+B}$	$\overline{A}\overline{B}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

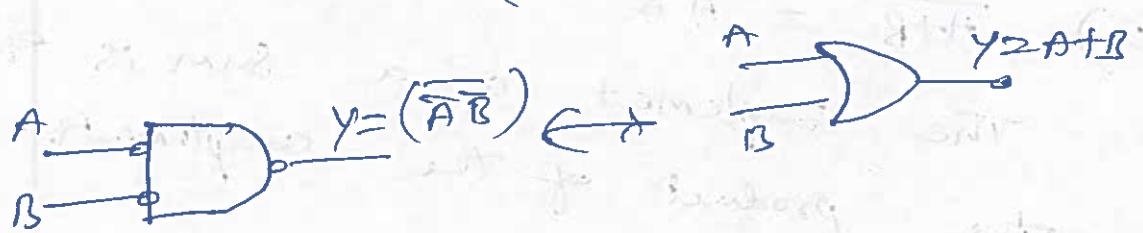
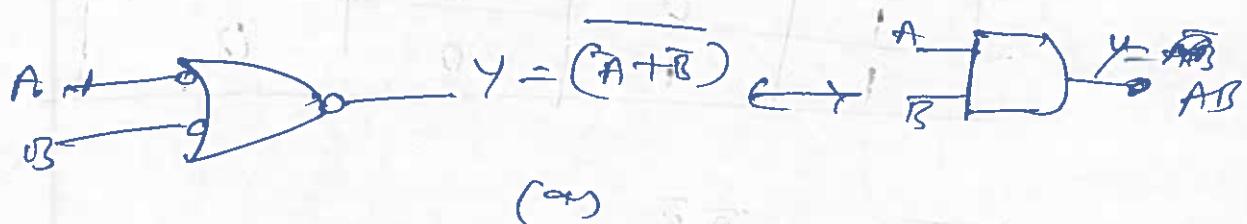
→ ~~NAND~~ and ~~NOR DTL gates~~

The "If and only if all inputs are true(1) then the output is true(1)" is logically equivalent to the statement "If at least one input is false(0), then the output is false(0)".

$$ABC = \overline{\overline{A} + \overline{B} + \overline{C}} \dots \text{---} \textcircled{1}$$

If we complement of the both sides of this equation

$$\overline{\overline{A} + \overline{B} + \overline{C}} \dots = \overline{ABC} \dots$$



NAND and NOR DTL gates

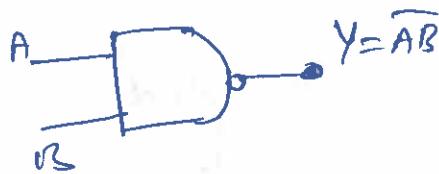
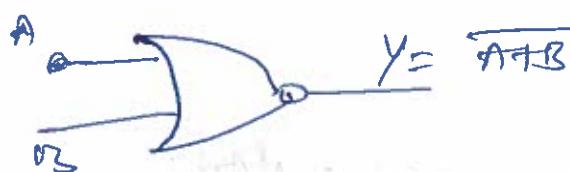


Fig (a)

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(b)

Fig (a) Two input NAND gate (b) Truth table



(a)

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(b)

Fig (b) Two input NOR gate and (b) Truth table

→ Negated AND is called a NOT-AND for NAND gate.  
 This is also called diode-transistor logic (DTL).

→ A negation following an OR is called a NOT-OR, or a NOR gate.

→ This is also called diode-transistor logic

ex: DTL circuit

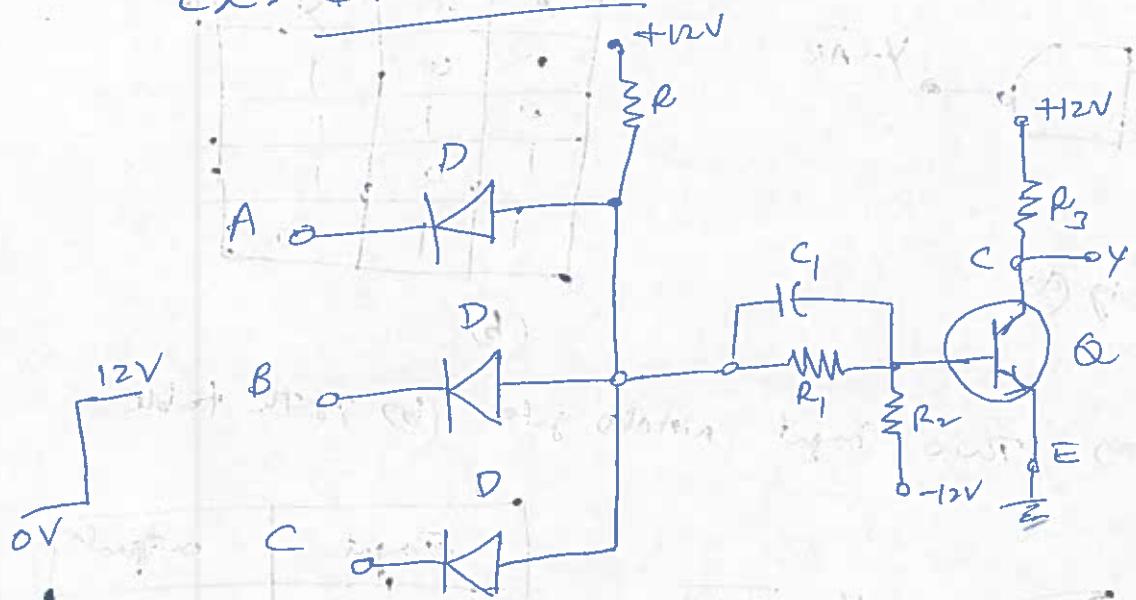
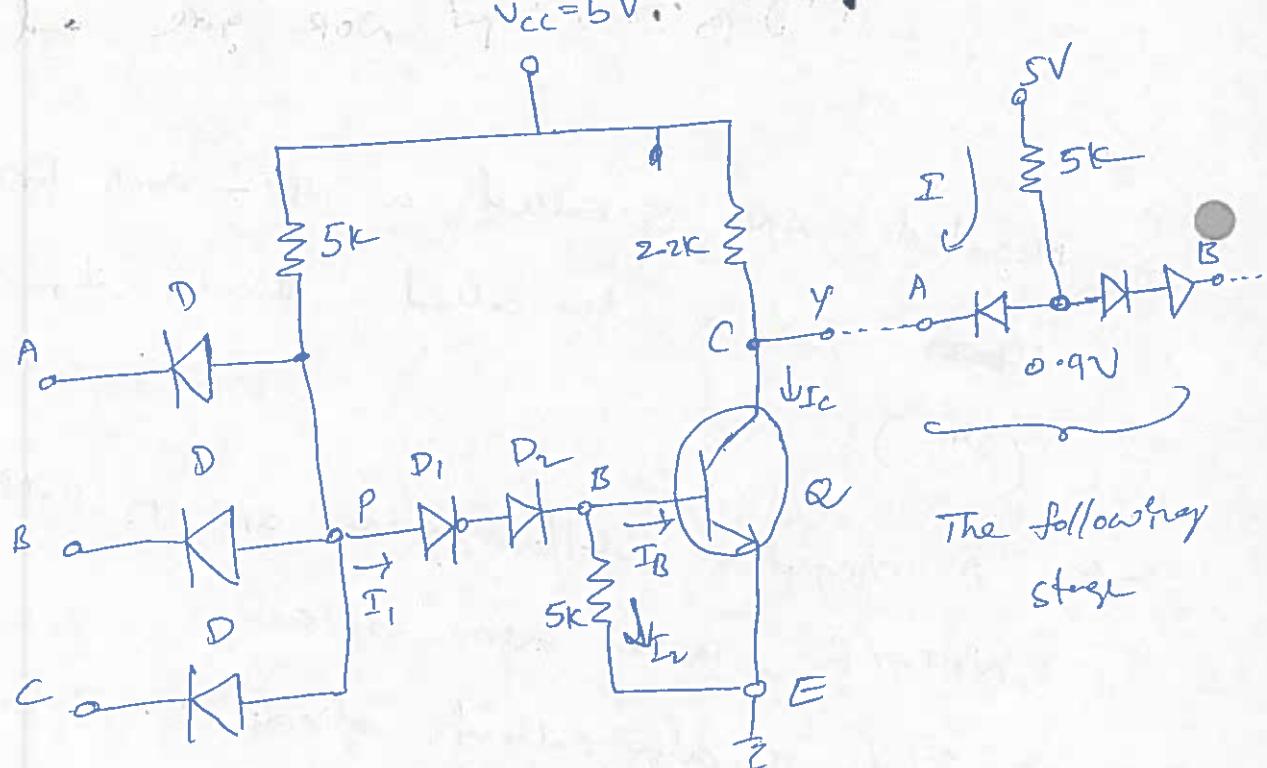


Fig.: A three input positive NAND gate.

→ modified (Integrated circuit) DTL gates.



The following stage

Fig.2: An Integrated positive DTL NAND gate

most logic gates are ~~fabricated~~ fabricated as an integrated circuit (IC).

fig ① is modified for integrated-circuit implementation by eliminating the capacitor  $C_1$ , reducing the resistance values, and using diodes or transistors to replace resistors wherever possible. At the same time the power-supply requirement is simplified so that only a single 5V supply is used. The resulting circuit is indicated in fig ②.

operation:  
If at least one of the inputs is low (the 0 state), the diode  $D$  connected to this input conducts and the voltage  $V_p$  at point  $p$  is low. Hence diodes  $D_1$  and  $D_2$  are non-conducting,  $I_B = 0$ , and the transistor is off. Therefore the output of  $\alpha$  is high and  $\gamma$  is in the 1 state. This logic satisfies the first three rows of the truth table.

All ~~the~~ inputs are high (1) so that all input diodes  $D$  are cut off, the  $V_p$  tries to

rise toward  $V_{CC}$ , and Base current  $I_B$  results.

If  $I_B$  is sufficiently large,  $\alpha$  is driven into saturation and the output  $y$  falls to its low(0) state, and satisfying the fourth row of the truth table.

→ High - Threshold - Logic (HTL) Gate:

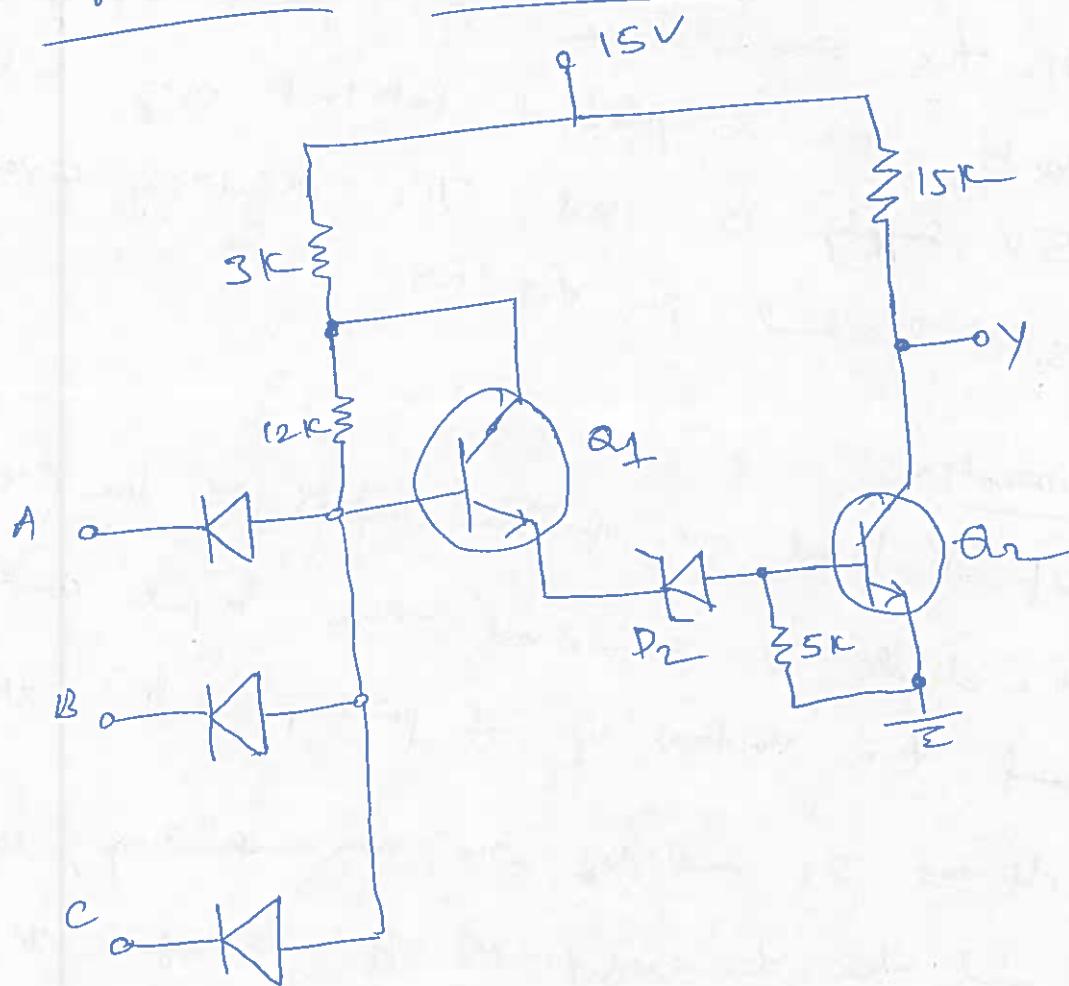


Fig: A high-threshold-logic NAND gate

In an industrial area the noise level is high because of the presence of motors, high voltage switches, on-off control circuits. By using a higher supply voltage ( $15V$  instead of  $5V$ ) and a  $6.9V$ -Zener diode in place of  $D_2$  in the  $DT_2$  gate of fig. This circuit is converted into the high noise immunity gate of fig. approximately the same currents are obtained in both  $\otimes$  circuits. The noise margin obtained with this circuit is typically  $7V$  (prob.  $6.4V$ ).

### → Transistor - Transistor - Logic (TTL) Gate

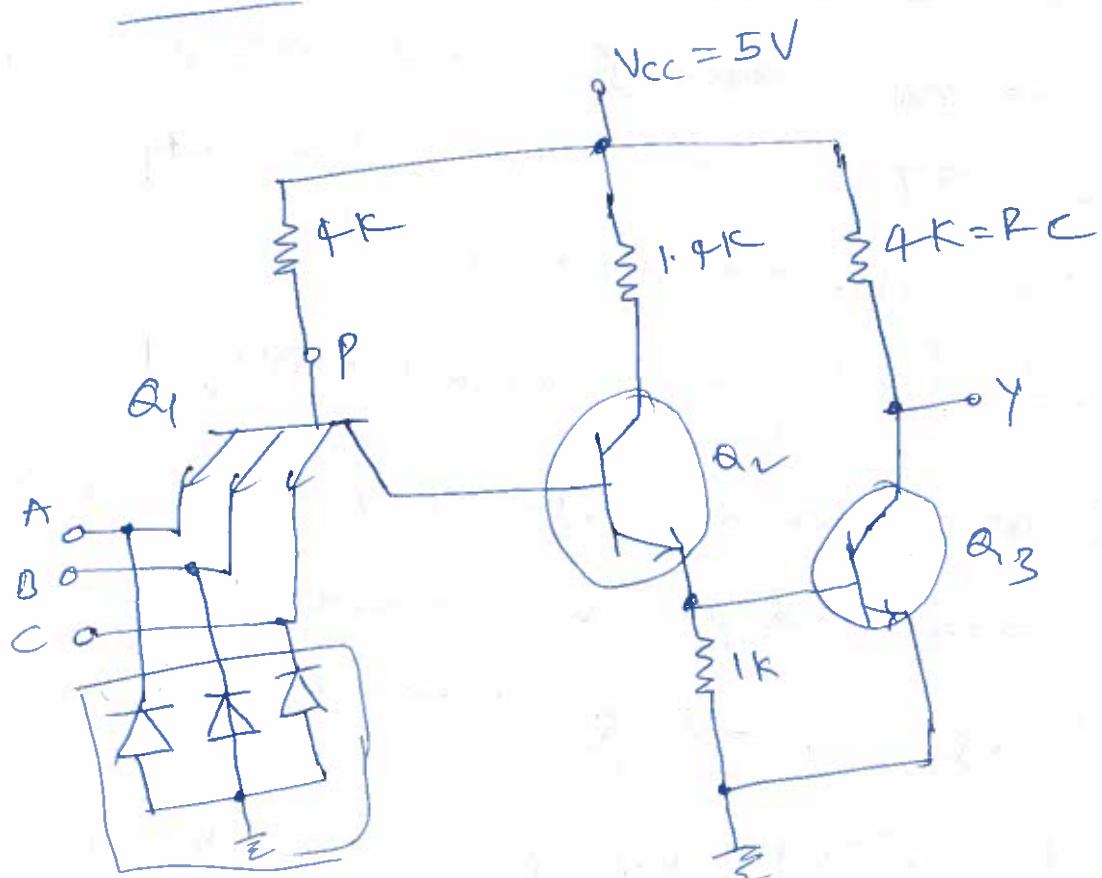


fig: An  $\text{fC}$  positive TTL NAND gate  
(Neglect the diodes in the shaded block)

The fastest-saturation logic circuit is the transistor-transistor logic gate (TTL, or T<sup>2</sup>L) as shown in fig.

This switch uses a multiple-emitter transistor as easily and economically fabricated using integrated-circuit techniques.

operation  
If at least one input is at  $V(0) = 0.2V$ ,

$$\text{then } V_p = 0.2 + 0.7 = 0.9V.$$

For the collector junction of  $Q_1$  to be forward-biased and for Q<sub>2</sub> and Q<sub>3</sub> to be on requires about  $0.7 + 0.7 = 2.1V$ . Hence these are off, the output goes to  $V_{cc} = 5V$ , and  $Y = 1$ .

If all inputs are high (at 5V), the input diodes (the emitter junctions) are reverse biased and  $V_p$  rises toward  $V_{cc}$ , and drives Q<sub>2</sub> and Q<sub>3</sub> into saturation. Then

$$\text{the output } V_{CE,\text{sat}} = 0.2V, \text{ and } Y = 0$$

## output stages!

At the output terminal of the DTL or TTL gate there is a capacitive load  $C_L$ , consisting of the capacitance of the reverse-biased diodes of the fan-out gates and any wiring capacitance.

If the collector-circuit resistor of the inverter is  $R_C$ , then, when the output changes

from the low to the high state, the output transistor is cut off and the capacitance charges exponentially from  $V_{CC}$ , set to  $V_{CC}$ .

The output delay may be reduced by

decreasing  $R_C$ . ✓

### The final stage

The final value of the output voltage

$$V_o = V_{CC} - V_{BEF, cutin} - V_{DQ, cutin} \approx 5 - 0.5 - 0.6 \\ = 3.9 \text{ V} \approx V_{CL}$$

✓

unit-3, 31/35

## Resistor-Transistor Logic (RTL)

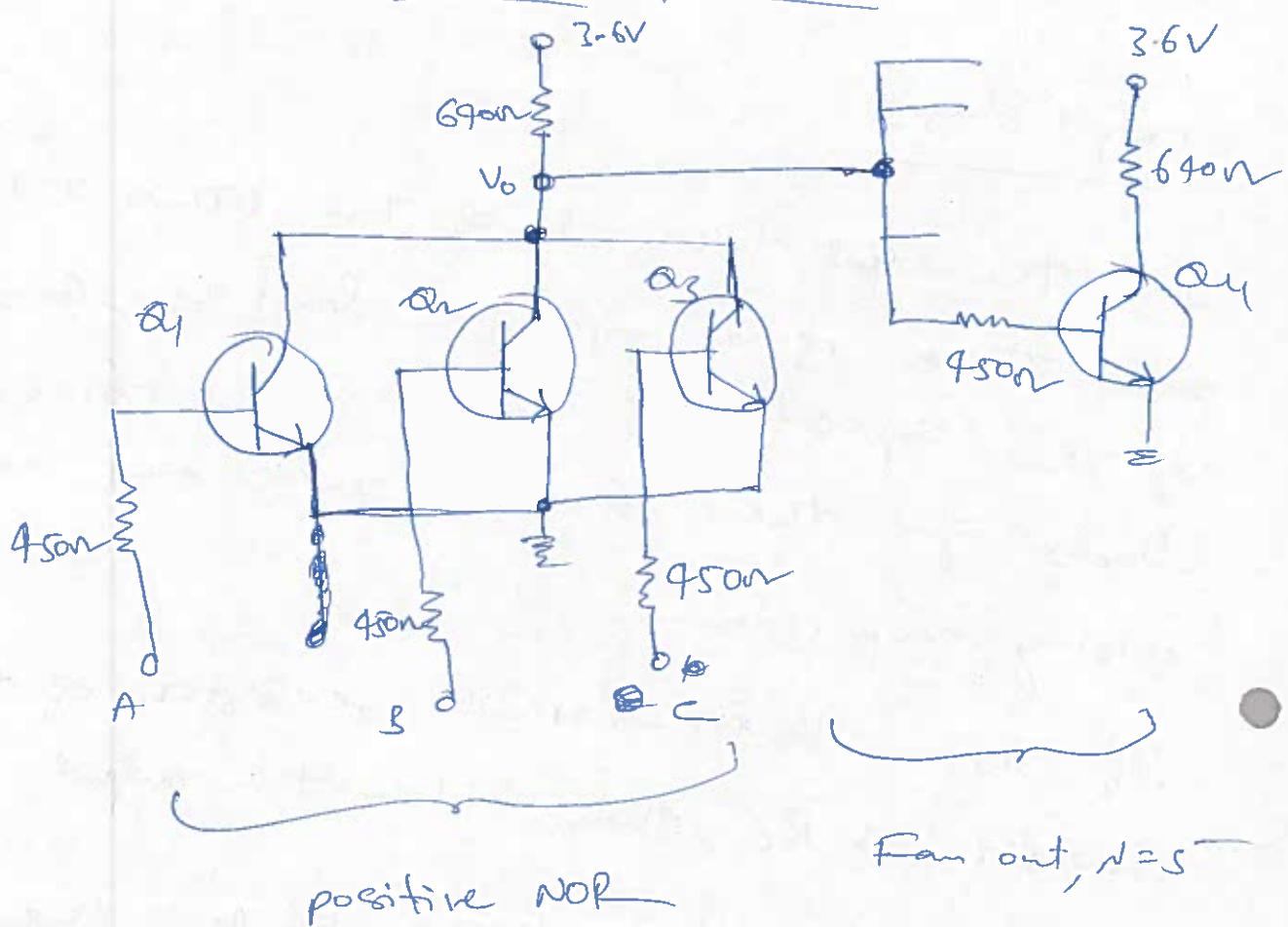


Fig. (a) An RTL positive NOR gate with a fan-in of 3 and a fan-out of 5.

If any input is high, the corresponding Transistor is driven to saturation and output is low ( $V_{o} = 0$ ).

If all inputs are low, then all input transistors are cut off and the output is high.

## Direct-coupled Transistor logic (DCTL)

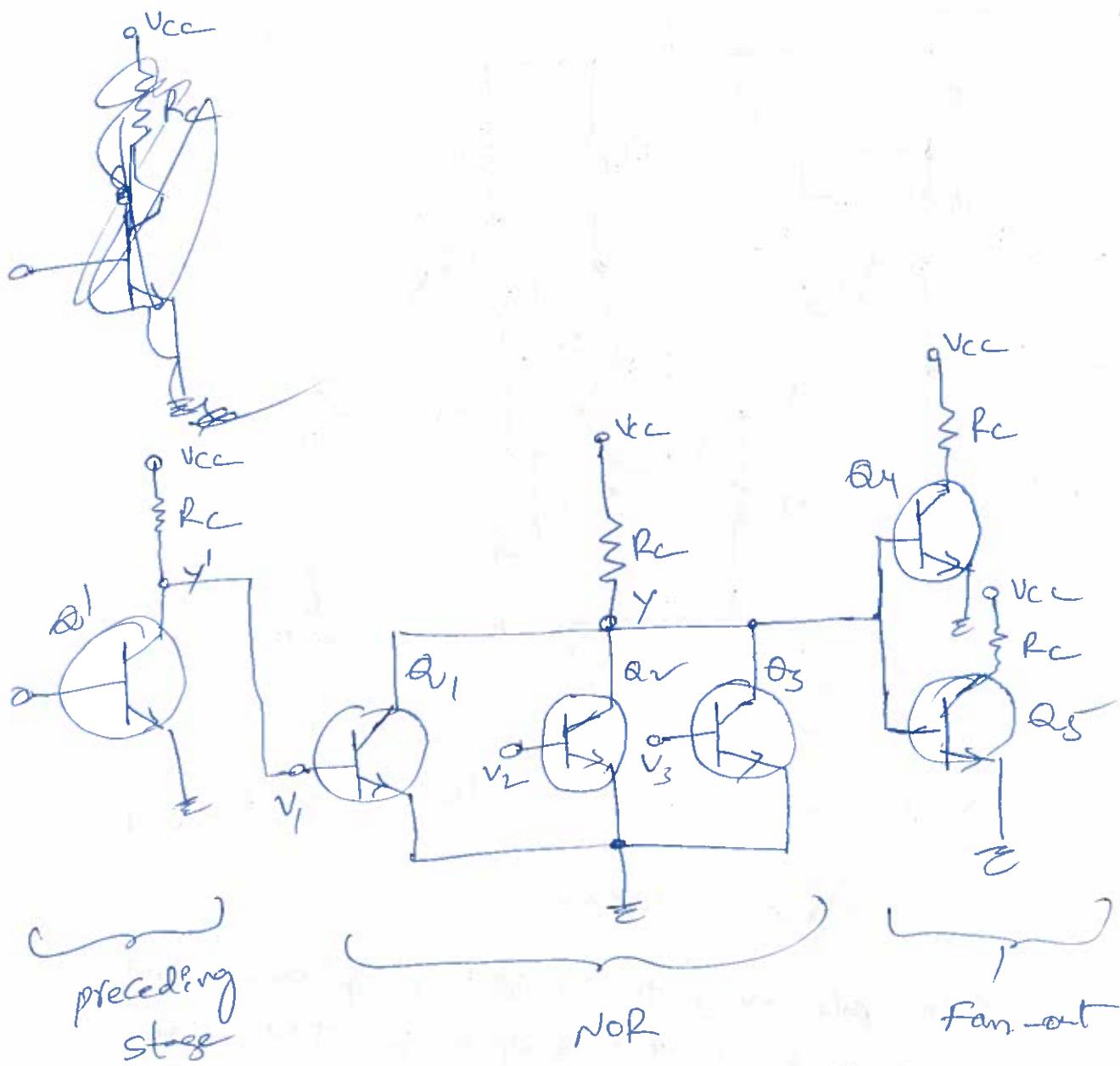


Fig: A positive NOR DCTL gate

This configuration is the same as RTL.

Fan in is 3 and fan out is 2.

With all inputs in the low state,  
the output is high.

At least one input is for the high state  
output is low state.

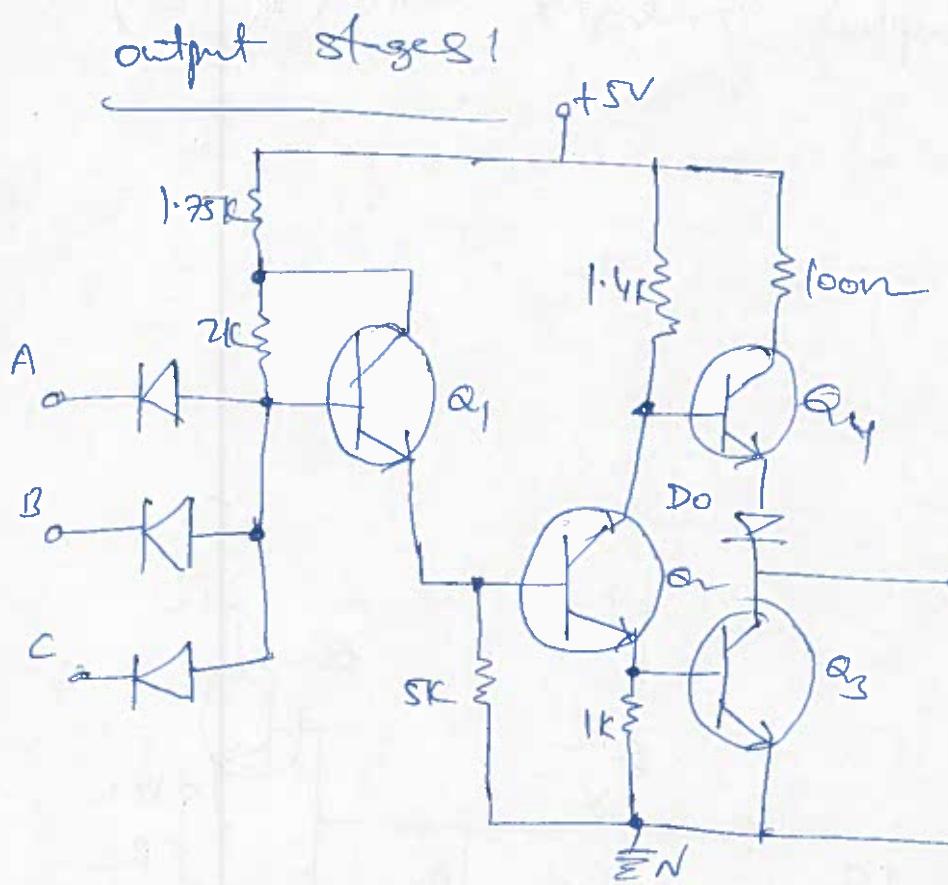


Fig. DTL gate with a totem-pole output driver.

Totem pole means the addition of an active pull UP the circuit for the output of the Gate, it's results for a reduction of propagation delay.

✓ output driver circuit use to convert one level of voltage into another level of voltage.

# Comparison of logic families

parameter	DTL	TTL	RTL	DCTL	CMOS	ECL
1. basic logic gate	ND ND	NAND	NOR	NAND	NOR, NAND	OR/NOR
2. components	Resistor Transistor & Diodes	Transistor & Register	Resistor & Transistor	Resistor & Transistor	pMOS nMOS	Resistor & Transistor
3. power dissipation	8-12 mW	10 mW	30 mW	30	0.1 (0.025-1.01 mW)	40-55 mW
4. propagation delay (ns)	30 nsec	10 nsec	12 nsec	10	70 nsec	2 nsec 1-2 ns
5. noise margin (noise immunity)	High (Good)	Medium (Very Good)	Poor (Nominal)	Poor	High (Very Good)	Low (Poor)
6. Fan out	medium(8)	High (10) (10-20)	low(4) (5)	Low(4)	High(50) (20-50)	very high (25)

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